

RAJASTHAN TECHNICAL UNIVERSITY

SYLLABUS: M.TECH (VLSI DESIGN)

1MVL1 ADVANCED MATHEMATICS

Optimization problem-Convex sets and functions.

The SIMPLEX Algorithm- Forms of linear programming problem, geometry of linear programming, Organization of Tableau. Computational considerations for SIMPLEX Algorithm.

Duality: Dual of linear programming, dual simplex problem, Primal-dual algorithm.

Algorithms and Complexity-shortest path, max-flow, Dijkstra's algorithm, min-cost flow, algorithm for graph search and matching; spanning trees and matroids; Integer Linear programming, Greedy algorithm, approximation algorithms; branch-and-bound; dynamic programming.

1MVL 2 VLSI DESIGN

Basic operation of CMOS inverter, detailed analysis of its noise margin propagation delay, power dissipation concept of layout & area, layout optimization & area estimation for a single as well as combinational logic circuits.

Design of sequential logic circuits: Static & dynamic latches registers, dynamic transmission gate, CMOS gate, pipelining approach for optimize sequential circuits, NDRA-CMOS pipelined structure, non-bistable sequential circuits, Schmitt trigger.

Implementation strategies for digital ICs, introduction of custom and circuit design, hierarchy cell based design array based implementation, building blocks of adder, multiplier, shifter, barrel shifter, algorithmic shifter and other arithmetic operators, power speed tradeoff in data path structure.

Design memory & array structure memory architectures & building blocks, address decoder, sense amplifiers, driver/ buffers, timing control, power dissipation in memories, idea of testability and fault detection models.

1MVL 3 DIGITAL SYSTEM DESIGN

Sequential Logic Design- Introduction, Basic Bistable Memory Devices, reduced characteristics and excitation table for bistable devices.

Synchronous Sequential Logic Circuit Design: Introduction, Moore, Mealy and Mixed type Synchronous State Machines. Synchronous sequential design of Moore, Mealy Machines, Synchronous Counter Design, Hazards, Duality of sequential circuits, Different methods of minimization.

Asynchronous Sequential logic design- Introduction, Primitive flow table and reduction, type of delays, Cycles and races, Excitation Map, Hazards, Essential hazards, Analysis of asynchronous sequential circuits.

Symmetric and Iterative circuits- Symmetric functions, iterative functions, realization in tree form.

Algorithmic State Machine: An Algorithm with inputs, digital solution, Implementation of traffic light controller, ASM charts, Design Procedure for ASMs.

Introduction to programmable logic devices: PALs, PLDs, CPLDs and FPGAs.

Introduction to VHDL: Data types, Concurrent statements, sequential statements, behavioral modeling.

2MVL 1 DIGITAL SIGNAL PROCESSING

DFT & its properties. Decimation in time and decimation in frequency FFT algorithms, discrete cosine transform.

IIR Filter design: Butterworth design, bilinear transformation. Low Pass, High Pass, Band Pass and Band Stop digital filters. Spectral transformation of IIR filters.

FIR filter design: Symmetric and antisymmetric linear phase. FIR filter by rectangular, triangular and Blackman window functions.

Finite word length effects in FIR and IIR digital filters: Quantization, round off errors and overflow errors.

Multi rate digital signal processing: Concepts, design of practical sampling rate converters, Decimators, interpolators. Polyphase decompositions.

2MVL 2 ANALOG & MIXED SIGNAL ICs

Review of BJT and MOS transistor operation, models and equivalent circuits, single-stage amplifiers, differential amplifiers. Passive and active current mirrors: Cascade current mirror, Wilson current mirror. Mismatch & nonlinearity.

Theory & design of MOS operational amplifiers, complete CMOS operational amplifier including frequency compensation, stability, frequency response and transient response.

Comparator & voltage reference sources.

Switches capacitor circuits: Principles of operation of switches, capacitor circuits, switched capacitor filters. D/A and A/D converter.

Nonlinear analog circuits: Timer, function generators, multipliers and PLL.

Bi CMOS: Devices & technology, basic analog & digital sub circuits, inverters.

2MVL 3 CAD of ICs

Introduction to concept of design, design methodologies, semi-custom and custom design approaches.

Data path & control design.

Elements of device and circuit simulation, logic simulation.

Stick diagram and representation, layout of ICs, lambda based design rules.

Deep submicron interconnects modeling and synthesis.

Topics in design-yield and redundancy, low power design techniques.

3MVL 1 EMBEDDED SYSTEM DESIGN

The concept of embedded systems design: definitions and constraints, hardware and processor requirements, embedded microcontroller cores, embedded memories. Examples of embedded systems.

Technological aspects of embedded systems: special purpose processors; input-output design and I/O communication protocols; design space exploration for constraint satisfaction; co-design approach; example system design, interfacing between analog and digital blocks, signal conditioning, digital signal processing. sub-system interfacing, interfacing with external systems, user interfacing. Design trade offs due to process compatibility, thermal considerations etc.

Software aspects of embedded systems: real time programming languages and operating systems for embedded systems. specification refinement and design; design validation; Real Time operating system issues with respect to embedded system applications; time constraints and performance analysis.

1MVL 4.1 LOW POWER VLSI DESIGN

Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power

Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

Simulation Power analysis:

SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation.

Probabilistic power analysis:

Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

Low Power Design

Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library

Logic level:

Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

Low power Architecture & Systems:

Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Low power Clock Distribution:

Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip and package co-design of clock network

Algorithm and architectural level methodologies:

Introduction, design flow, algorithmic level analysis and optimization, Architectural level estimation and synthesis.

1MVL 4.2 MICRO-ELECTRO-MECHANICAL-SYSTEMS (MEMS)

Micro electro mechanical system (MEMS) origins. MEMS impetus/ motivation. Material for MEMS. The toolbox: processes for micro machining. MEMS fabrication technologies. Fundamentals MEMS device physics: Actuation. Fundamental MEMS devices: The cantilever beam. Microwave MEMS applications: MEM switch design considerations. The micro-machined transmission line. MEMS-based microwave circuit and system.

1MVL 4.3 MICROELECTRONICS

Introduction to semiconductor physics: Review of quantum mechanics, electrons in periodic lattices, E-k diagrams, Quasi-particles in semiconductors, electrons, holes and phonons. Boltzmann transport equation and solution in the presence of low electric and magnetic fields - mobility and diffusivity; carrier statistics; continuity equation, poisson's equation and their solution; high field effects: velocity saturation, hot carriers, avalanche breakdown, punch through and kirk effects.

Semiconductor junctions: Schottky, homo- and hetero-junction band diagrams and I-V characteristics, small signal switching models; two terminal and surface states devices based on semiconductor junctions.

Bipolar transistor working, its charge control, and gummel poon model, structure of graded base, graded emitter transistor, hetro junction transistor.

MOS structures: Semiconductor surfaces; the ideal and non ideal MOS capacitor band diagrams and CVs; Effects of oxide charges, defects and interface states; characterization of MOS capacitors: HF and LF CVs, avalanche injection; high field effects and breakdown. Long & short channel effects.

2MVL 4.1 HIGH LEVEL SYSTEM DESIGN & MODELING

System level design, description languages- SDL, SpecChart etc.

Architectural synthesis for DSP applications.

Formal Verification of digital systems- BDD based approaches, functional equivalence, finite state automata, ω -automata, FSM verification.

Hardware-software partitioning, interface synthesis, case studies.

2MVL 4.2 FPGA BASED SYSTEM DESIGN

Evolution of programmable devices: Introduction to AND-OR structured Programmable Logic Devices PROM, PLA, PAL and MPGAs; Combinational and sequential circuit realization using PROM based Programmable Logic Element (PLE); Architecture of FPAD, FPLA, FPLS and FPID devices.

FPGA Technology: FPGA resources - Logic Blocks and Interconnection Resources; Economics and applications of FPGAs; Implementation Process for FPGAs Programming Technologies - Static RAM Programming, Anti Fuse Programming, EPROM and EEPROM Programming Technology; Commercially available FPGAs - Xilinx FPGAs, Altera FPGAs; FPGA Design Flow Example - Initial Design Entry, Translation to XNF Format, Partitioning, Place and Route, Performance Calculation and Design Verification.

Technology Mapping for FPGAs: Logic Synthesis - Logic Optimization and Technology Mapping; Lookup Table Technology Mapping - Chortle-crf Technology Mapper, Chortle-d Technology Mapper, Lookup Table Technology Mapping in mis-pga, Lookup Table Technology Mapping in Asyl and Hydra Technology Mapper; Multiplexer Technology Mapping - Multiplexer Technology Mapping in mis-pga.

Routing for FPGAs: Routing Terminology; Strategy for routing in FPGAs; Routing for Row- Logic Block Architecture: Logic Block Functionality versus Area-Efficiency - Logic Block Selection, Experimental Procedure, Logic Block Area and Routing Model and Results.

Based FPGAs - Segmented channel routing, 1-channel routing algorithm, K - channel routing algorithm and results.

2MVL 4.3 BIOMEDICAL ELECTRONICS

Brief introduction to human physiology. Biomedical transducers: displacement, velocity, force, acceleration, flow, temperature, potential, dissolved ions and gases.

Bioelectrodes and biopotential amplifiers for ECG, EMG, EEG, etc. Measurement of blood temperature, pressure and flow. Impedance plethysmography. Ultrasonic and nuclear imaging.

Prostheses and aids: pacemakers, defibrillators, heart-lung machine, artificial kidney, aids for the handicapped. Safety aspects.

Telemetry - Transmission of the original through wire & wireless.

Imaging techniques - Ultrasound, CAT, X-Rays, PET, NMR, Nuclear.

Physiological effect of electric current, safety.

Cardiological Signal Processing: Basic Electrocardiography, ECG data acquisition, ECG lead system, ECG parameters & their estimation, the use of multi scale analysis for parameters estimation of ECG waveforms, Arrhythmia analysis, monitoring, long form continuous ECG recording.

ECG data reduction technique, Direct data compression techniques, Direct ECG data compression techniques. Transformation compression techniques. Other data compression techniques. Data compression techniques, comparison.

3MVL 2.1 VLSI TESTING & TESTABILITY

Physical Faults and their modeling; Stuck at Faults, Bridging Faults; Fault collapsing; Fault Simulation: Deductive, Parallel, and Concurrent Fault Simulation.

Critical Path Tracing;

ATPG for Combinational Circuits: D-Algorithm, Boolean Differences, PODEM Random, Deterministic and Weighted Random Test Pattern Generation; Aliasing and its effect on Fault Coverage.

PLA Testing, Cross Point Fault Model and Test Generation.

Memory Testing Permanent Intermittent and Pattern Sensitive Faults, Marching Tests; Delay Faults.

ATPG for Sequential Circuits : Time Frame Expansion ; Controllability and Observability Scan Design, BILBO , Boundary Scan for Board Level Testing ; BIST and Totally self checking circuits.

System Level Diagnosis: Introduction; Concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction Codes.

Reconfiguration Techniques; Yield Modeling, Reliability and effective area utilization.

3MVL 2.2 NANOELECTRONICS

Shrink-down approaches: Introduction, CMOS scaling, the nanoscale MOSFET, finfets, vertical MOSFETs, limits to scaling, system integration limits (interconnect issues etc.), resonant tunneling transistors, single electron transistors, new storage, optoelectronic, and spintronics devices. Atoms-up approaches: Molecular electronics involving single molecules as electronic devices, transport in molecular structures, molecular systems as alternatives to conventional electronics, molecular interconnects; Carbon nanotube electronics, bandstructure & transport, devices, MEMS applications.

3MVL 2.3 ADVANCE IC TECHNOLOGY AND CHARACTERIZATION TECHNIQUES

INTRODUCTION

Tools for technological processing in microelectronics. survey of methods for analysis of microelectronic materials and devices. Classification of different tools for bulk , surface and thin film characterization.

FABRICATION OF NANOSCALE AND SUBMICRON STRUCTURES

Physical and chemical techniques for nanomaterial synthesis, Assembling and self organization of nanostructures, Nanoscale manipulation, Nanotube and wire formation ,Importance of size distribution control, size measurement and size selection.

Fabrication of hetrostructure in submicron and quantum level for microelectronic and optical applications

VARIOUS CHARACTERISATION TECHNIQUES

Theory and working principle of XRD, SEM , IR, RHEED ,LEED, XPS, AFM ,STM .working of thermal, optical and electrical measurement techniques'

1MVL 5 VLSI PHYSICAL DESIGN LAB

PART A

Draw the Layout, do circuit partitioning , placement and routing, circuit compaction, check DRC , Circuit extraction and finally post layout simulation for different combinational and sequential circuits.

PART B

Use the feature of automation test program generation, multilevel logic synthesis for design smaller application chips like multi bit parallel adder priority encoder, general purpose register, ALU, microcontroller/ dsp processor/ traffic light controller /sequential adder etc.

2MVL 5 DIGITAL SYSTEM DESIGN LAB

Design ,implement and experiment with digital system, this will include ASIC design, FPGA based design. design of relevant hardware and software for microcontroller ,processor and DSP based embedded system.

Custom design and simulation of different higher level analog and digital circuits using advance EDA tools like Tanner Spice S-edit and L- edit